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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,290	07/27/2001	Faraydon O. Karim	00-LJ-217 (STMI01-00217)	8101

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,290	KARIM ET AL.	
	Examin r	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on th cover sheet with the correspond nc addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined. Claims 1-3, 5, 8-10, 12, and 15-17 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment and Extension of Time as received on 20 September 2004.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boufarah et al., U.S. Patent No. 5,127,091 (herein referred to as Boufarah) in view of Ekner, U.S. Patent Number 6,289,445 (herein referred to as Ekner).

5. Regarding claims 1, 8 and 15, taking claim 8 as exemplary, Boufarah has taught a processor comprising:

a. At least one execution unit (Boufarah 20 of Fig.1),

b. A decode unit (Boufarah 20 of Fig.1, see Col.3 line 61 – Col.4 line 22),

c. A branch architecture for limiting branch penalty without branch prediction comprising:

i. A fetch-branch unit (Boufarah 14 of Fig.1) operating in parallel with the decode unit (Boufarah Fig.1) and controlling retrieval of instructions for

the decode unit (Boufarah Col.3 lines 34-38), wherein the fetch-branch unit, upon detecting a branch instruction during one cycle,

(1) Initiates retrieval of at least one sequential instruction from a location immediately following a location of a last retrieved instruction during one of a first cycle immediately following the one cycle and a second cycle immediately following the first cycle (Boufarah Col.7 lines 33-54, as well as Fig.2c, Fig.2d and Col.4 line 29 – Col.5 line 19),

(2) Initiates retrieval of at least one target instruction from a target location for the branch instruction during the other of the first cycle immediately following the one cycle and the second cycle immediately following the first cycle (Boufarah Col.7 lines 33-54, as well as Fig.2c, Fig.2d and Col.4 line 29 – Col.5 line 19).

6. Boufarah has not taught both the fetch-branch unit and the decode unit receiving the same instruction(s) during a given cycle. Ekner has taught both the fetch-branch unit and the decode unit receiving the same instruction(s) during a given cycle (Ekner column 5, line 52 to column 6, line 4 and Figure 2). A person of ordinary skill in the art at the time the invention was made would have recognized that the pipeline of Ekner, which determines the branch addresses and sends them for fetching at the same time as decoding the instruction, overlaps execution, thereby improving efficiency and execution speed of the CPU (Ekner column 5, lines 37-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was

made to incorporate the pipeline with a fetch-branch unit and decoder in the same stage, as taught by Ekner, in the device of Boufarah to improve efficiency and execution speed.

7. Claims 1 and 15 are nearly identical to claim 8. Claim 1 differs in its lack of execution and decode units, but encompasses the same scope as claim 8. Claim 15 differs in it being comprised in a method, but encompasses the same scope as claim 8. Therefore, claims 1 and 15 are rejected for the same reasons as claim 8.

8. Regarding claims 2, 9 and 16, taking claim 9 as exemplary, Boufarah in view of Ekner has taught the processor as set forth in claim 8, wherein the fetch-branch unit resolves the branch instruction and, upon resolving the branch instruction (Boufarah Col.7 line 55 – Col.8 line 9), causes both the fetch-branch unit and the decode unit (Ekner column 5, line 52 to column 6, line 4 and Figure 2) to drop either the at least one sequential instruction or the at least one target instruction (Boufarah Col.7 line 55 – Col.8 line 9).

9. Claims 2 and 16 are nearly identical to claim 9, differing only in their parent claims, but encompassing the same scope as claim 9. Therefore, claims 2 and 16 are rejected for the same reasons as claim 9.

10. Regarding claims 3, 10 and 17, taking claim 10 as exemplary, Boufarah in view of Ekner has taught the processor as set forth in claim 9, wherein the fetch-branch unit, upon resolving the branch instruction (Boufarah Col.7 line 55 – Col.8 line 9), initiates retrieval to both the fetch-branch unit and the decode unit (Ekner column 5, line 52 to column 6, line 4 and Figure 2) of at least one instruction from a location immediately following a location of a last retrieved instruction within either the at least one sequential instruction or the at least one target instruction, depending upon whether a branch is taken (Boufarah Col.7 line 55 – Col.8 line 9).

11. Claims 3 and 17 are nearly identical to claim 10, differing only in their parent claims, but encompassing the same scope as claim 10. Therefore, claims 3 and 17 are rejected for the same reasons as claim 10.

12. Regarding claims 4, 11 and 18, taking claim 11 as exemplary, Boufarah in view of Ekner has taught the processor as set forth in claim 9, wherein the fetch-branch unit, upon detecting a branch instruction during the one cycle, marks any fetched instruction preceding the branch instruction with a regular instruction type identifier (Boufarah "X1, X2" of Fig.2h), marks the branch instruction with a branch instruction type identifier (Boufarah "BRC" of Fig.2h), and marks any fetched instruction succeeding the branch instruction with a sequential instruction type identifier (Boufarah "S1, S2, S3" of Fig.2h). Here, while the processor of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (Boufarah Col.5 line 61 – Col.6 line 39).

13. Claims 4 and 18 are nearly identical to claim 11, differing only in their parent claims, but encompassing the same scope as claim 11. Therefore, claims 4 and 17 are rejected for the same reasons as claim 11.

14. Regarding claims 5, 12 and 19, taking claim 12 as exemplary, Boufarah in view of Ekner has taught the processor as set forth in claim 11, wherein the fetch-branch unit, upon not detecting a branch instruction during the one cycle, marks all fetched instruction(s) with the regular instruction type identifier (Boufarah "X1, X2, X3" of Fig.2j). Here, while the processor

of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (Boufarah Col.6 line 40 – Col.7 line 13).

15. Claims 5 and 19 are nearly identical to claim 12, differing only in their parent claims, but encompassing the same scope as claim 12. Therefore, claims 5 and 19 are rejected for the same reasons as claim 12.

16. Regarding claims 6 and 13, taking claim 13 as exemplary, Boufarah in view of Ekner has taught the processor as set forth in claim 8, wherein the fetch-branch unit marks the at least one sequential instruction with a sequential type identifier (Boufarah "S1, S2, S3" of Fig.2h). Here, while the processor of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (Boufarah Col.5 line 61 – Col.6 line 39).

17. Claim 6 is nearly identical to claim 13, differing only in its parent claim, but encompassing the same scope as claim 13. Therefore, claim 6 is rejected for the same reasons as claim 13.

18. Regarding claims 7 and 14, taking claim 14 as exemplary, Boufarah in view of Ekner has taught the processor as set forth in claim 8, wherein the fetch-branch unit marks the at least one target instruction with a target instruction type identifier (Boufarah "T1, T2, T3, T4" of Fig.2h).

Here, while the processor of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (Boufarah Col.5 line 61 – Col.6 line 39).

19. Claim 7 is nearly identical to claim 14, differing only in its parent claim, but encompassing the same scope as claim 14. Therefore, claim 7 is rejected for the same reasons as claim 14.

20. Regarding claim 20, Boufarah in view of Ekner has taught the method as set forth in claim 15, further comprising:

a. Marking the at least one sequential instruction with a sequential instruction type identifier (Boufarah "S1, S2, S3" of Fig.2h),

b. Marking the at least one target instruction with a target instruction type identifier (Boufarah "T1, T2, T3, T4" of Fig.2h). Here, while the processor of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (see Col.5 line 61 – Col.6 line 39).

Response to Arguments

21. Examiner withdraws 35 U.S.C. § 112, second paragraph rejection withdrawn in favor of amended claims.

22. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
21 December 2004

RICHARD L. ELLIS
PRIMARY EXAMINER